Please add the following new claims 12 and 13.

figs. 14, 15 G5 C1

-- 12. The semiconductor device of claim 1, wherein the fourth region is a continuous region having changing depths in a direction crossing a direction of current flow.

13. The semiconductor device of claim 7, wherein the fourth region is a continuous region having changing depths in a direction crossing a direction of current flow.

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REMARKS

This Amendment is being filed in response to the Office Action dated March 13, 2002. For the following reasons, this Application should be allowed, and the case passed to issue.

No new matter is introduced by this amendment. The amendments to claims 1 and 5 are supported by the specification at page 10, lines 1-6, and FIG. 3. The amendment to page 10 of the specification is supported by page 6, lines 9-19 and originally filed claims 6 and 11. The amendment to page 16 of the specification is supported by originally filed claim 4. New claims 12 and 13 are supported by FIG. 14 and 15 and page 23, line 31 to page 24 line 5 of the specification.

Specification

The title is objected to as not being descriptive. Applicant submits that the new title is clearly indicative of the invention to which the claims are drawn.

The disclosure is objected to because the paragraph on page 6, lines 9-19 is allegedly unclear. Apparently, the Examiner is referring to the differences between this

paragraph and the paragraph starting at line 19 of page 10, as originally filed. This objection is traversed. Obvious typographical errors have been corrected in the paragraph starting at line 19 of page 10. Page 10 is now consistent with page 6 of the disclosure and claims 6 and 11.

The disclosure is further objected to because depletion layers C and D were not depicted in FIG. 28 and 29. This objection is traversed, and reconsideration and withdrawal respectfully requested. Corrected Figures 28 and 29, in which depletion layers C and D are clearly shown, have been filed in a separate paper.

Claim Rejections Under 35 U.S.C. § 112

Claims 4-11 are rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to make and/or use the invention. This rejection is traversed, and reconsideration and withdrawal respectfully requested.

The Examiner asserts that the written description does not disclose that the fourth region is electrically connected to the first electrode portion as claimed in claim 4. However, the paragraph beginning at line 28 of page 16 of the specification, as amended, provides support for claim 4. Applicant notes that the claims as originally filed are part of the disclosure.

OK

The Examiner furhter asserts that the written description does not disclose that the fourth regions are also formed discretely and the neighboring fourth regions are spaced from each other by a distance allowing connection between depletion layers extending

from the neighboring fourth regions, respectively, in an on state in the same embodiment of claim 1, as claimed in claim 5. Furthermore, the Examiner avers that the written description does not disclose the fourth region having a depth changing as the position moves in a direction crossing a direction of flow of the current, as claimed in claim 7.

As regards the rejection of claims 5 and 7, claims 1 and 5 have been amended so that they are now consistent with each other. The figures clearly show the fourth region comprises a plurality of discretely formed neighboring regions 7 and the **fourth region depletion layer B** has a depth changing as a position moves in a direction crossing a direction of flow of the current. Claim 7 reads on the sixth and eighth embodiments as described on page 19, line 1 to page 20, line 19; and page 21, line 20 to page 21, line 16.

OK

OK

In addition, the Examiner states that the written description does not disclose that the fourth region is electrically connected to the second electrode portion, as claimed in claim 9. Contrary to the Examiner's assertion, claim 9 is supported by Figures 26, 27, and 29, and the accompanying portions of the specification.

not true

Claims 5, 6, and 11 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite. This rejection is traversed, and reconsideration and withdrawal thereof respectfully requested.

The Examiner asserts that "said fourth regions" in line 2 of claim 5 has no antecedent basis and that claims 6 and 11 are unclear because of the uncertainty over the impurity concentration N_A and N_D.

These informalities have been corrected by the amendments to claim 5 and the specification. Applicant submits that the claims now fully comport with the requirements of 35 U.S.C. § 112.

Claim Rejections Under 35 USC § 103

Claims 1-6 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kitamura et al. (US Patent No. 5,432,370). This rejection is traversed, and reconsideration and withdrawal thereof respectfully requested. The following is a comparison between the invention as claimed and the cited prior art.

An aspect of the invention, per claim 1, is a semiconductor device comprising a semiconductor substrate of a first conductivity type and a first region of a second conductivity type formed on and in direct contact with the semiconductor substrate. A second region of the second conductivity type is formed at and near the surface of the first region. A third region of the first conductivity type, surrounding the second region, is formed at and near the surface of the first region. A first electrode portion is formed on the surface of the third region located between the first and second regions with an insulating film therebetween. A second electrode portion is connected to the second region. A third electrode portion is connected to the first region and spaced by a distance from the third region and a fourth region of the first conductivity type is formed at and near the surface of the first region between the third electrode portion and the third region. In an on state, a depletion layer extends from the fourth region. The depletion layer has a depth changing as a position moves in a direction crossing a direction of flow of the current.

The Examiner avers that Kitamura substantially teaches the claimed semiconductor device and that it would have been obvious to have a fourth region with a depth changing as the position moves in a direction crossing a direction of flow of the current because the formation of conductivity regions by the impurity diffusion method is widely used.

Kitamura does not teach a depletion layer extending from the fourth region having a depth changing as a position moves in a direction crossing a direction of flow of the current as required claim 1. Rather, Kitamura teaches (FIG. 6(a) and 6(b)) that region 4, through which current flows, has an impurity concentration higher than region 36. The depletion layer extends toward a region having lower impurity concentration. The depletion layer extending from the fourth region extends toward the region 2 side including region 2 located in region 36. Thus, Kitamura does not teach that the depletion layer extending from the fourth region has changing depths in the direction crossing the direction of current flow.

not OK

This rejection is improper and should be withdrawn. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge readily available to one of ordinary skill in the art. *In re Kotzab*, 217 F.3d 1365, 1370 55 USPQ2d 1313, 1317 (Fed. Cir. 2000); *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). There is no suggestion in Kitamura to provide a semiconductor device with a depletion layer extending from the fourth region that has changing depths in the direction crossing the

direction of current flow, as required by claim 1. The mere fact that references can be combined or modified does not render the resulting combination obvious unless the prior art also suggests the desirability the modification. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990).

The requisite motivation to support the ultimate legal conclusion of obviousness under 35 U.S.C. § 103 is not an abstract concept, but must stem from the applied prior art as a whole and realistically impel one having ordinary skill in the art to modify a specific reference in a specific manner to arrive at a specifically claimed invention. *In re Deuel*, 51 F.3d 1552, 34 USPQ2d 1210 (Fed. Cir. 1995); *In re Newell*, 891 F.2d 899, 13 USPQ2d 1248 (Fed. Cir. 1989). Accordingly, the Examiner is charged with the initial burden of identifying a source in the applied prior art for the requisite realistic motivation. *Smiths Industries Medical System v. Vital Signs, Inc.,* 183 F.3d 1347, 51 USPQ2d 1415 (Fed. Cir. 1999); *In re Mayne*, 104 F.3d 1339, 41 USPQ2d 1449 (Fed. Cir. 1997). There is no motivation in Kitamura for providing a semiconductor device in which a depletion layer extending from the fourth region has changing depths in the direction crossing the direction of current flow.

The only teaching of the claimed device, including the depletion layer extending from the fourth region that has changing depths in the direction crossing the direction of current flow is found in Applicant's disclosure. However, the teaching or suggestion to make a claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). The Examiner's conclusion of obviousness is not supported by any factual evidence. The Examiner's retrospective assessment of the

claimed invention and use of unsupported conclusory statements are not legally sufficient to generate a case of *prima facie* obviousness. The motivation for modifying the prior art must come from the prior art and must be based on facts.

Dependent claims 1-6 are allowable for at least the same reasons as claim 1. In addition, dependent claims 1-6 further distinguish the claimed invention. For example, claim 2 further requires a fifth region of the first conductivity type surrounding the third electrode portion, and formed at and near the surface of the first region. Claim 5 further requires that the fourth region comprises a plurality of discretely formed neighboring regions, and the neighboring fourth regions are spaced from each other by a distance allowing connection between depletion layers extending from the neighboring fourth regions, respectively, in an on state. Kitamura does not teach the claimed semiconductor device with these additional limitations.

As regards claim 2, the Examiner concludes that a fifth region of a first conductivity type surrounding the third electrode portion would be obvious because IGBT is a widely used power device in the power device family. As regards claims 5 and 6, the Examiner merely asserts these claims would have been obvious because the claimed configurations depend on the design of the device. The Examiner's conclusions, however, are not supported by any teaching in Kitamura. Thus, the conclusion of obviousness is not legally sufficient to support a case of *prima facie* obviousness and should be withdrawn.

Applicant submits that claims 7-11 are allowable as they have not been rejected with prior art and the rejections under 35 U.S.C. § 112 have been overcome in this

response. Applicant further submits new claims 12 and 13 are allowable, as they are dependent on allowable independent claims.

In light of the amendment and remarks above, this application is in condition for allowance and the case should be passed to issue. If there are any question regarding this Amendment or the application in general, a telephone call to the undersigned would be appreciated to expedite the prosecution of the application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The paragraph beginning at page 10, line 19 has been amended as follows:

Assuming that N^--type epitaxial layer 2 has an impurity concentration of [N_D] N_A, P-type diffusion region 7 has an impurity concentration of [N_A] N_D, neighboring P-type diffusion regions 7 are spaced by a distance of W, a required breakdown voltage is V, an amount of charges is q, a dielectric constant of the vacuum is ε, a relative dielectric constant of silicon is ε', and impurity concentration [N_A] N_D of P-type diffusion region 7 is sufficiently larger than impurity concentration [N_D] N_A of N^--type epitaxial layer 2, and is substantially infinite, the following formulas must be satisfied.

$$V > qN_DW^2/(8\varepsilon\varepsilon')$$

$$W < 2(2V\varepsilon\varepsilon'/(qN_D))^{(1/2)}$$

As shown in Fig. 3, the distance W between neighboring P-type diffusion regions 7 satisfies the foregoing relationships, whereby rising of the on resistance in the on state can be suppressed while keeping the effect of reducing the electric field.

The paragraph beginning at page 16, line 28, has been amended as follows:

In this semiconductor device, each P-type diffusion region 7 is fixed to the source potential. In particular, as shown in Fig. 23, each P-type diffusion region 7 is electrically connected to source electrode 9 via a contact hole 15, which is formed in silicon oxide film 20 and exposes the surface of corresponding P-type diffusion region 7. In alternative embodiments, each P-type diffusion region 7 is electrically connected to gate electrode 8a. Structures other than the above are substantially the same as those of the semiconductor

device shown in Fig. 1. The same parts and portions bear the same reference numbers, and description thereof is not repeated.

IN THE CLAIMS:

Claim 1 has been amended as follows:

1. (Amended) A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a first region of a second conductivity type formed on and in direct contact with said semiconductor substrate;

a second region of the second conductivity type formed at and near the surface of said first region;

a third region of the first conductivity type formed at and near the surface of said first region, and surrounding said second region;

a first electrode portion formed on the surface of said third region located between said first and second regions with an insulating film therebetween;

a second electrode portion connected to said second region;

a third electrode portion connected to said first region and spaced by a distance from said third region; and

a fourth region of the first conductivity type formed at and near the surface of said first region between said third electrode portion and said third region;

wherein, in an on state a depletion layer extends from said fourth region, and

said [fourth region] depletion layer having a depth changing as a position moves in a direction crossing a direction of flow of the current.

Claim 5 has been amended as follows:

5. (Amended) The semiconductor device according to claim 1, wherein said fourth [regions are formed discretely] region comprises a plurality of discretely formed neighboring regions, and

the neighboring fourth regions are spaced from each other by a distance allowing connection between depletion layers extending from the neighboring fourth regions, respectively, in [an] the on state.